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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS:	Stengel et al.	SERIAL NO.:	10/036,550
PATENT NO.:	6,819,181 B2	FILED:	12/21/2001
ISSUED:	11/16/2004	DOCKET NO.:	CM03422J
ENTITLED:	A METHOD AND STRUCTURE FOR INTEGRATED CIRCUIT INTERFERENCE ISOLATION ENHANCEMENT		

Certificate of Mailing

Date of deposit: February 14, 2005

I hereby certify that this paper is being deposited with the United States Postal Service on the date indicated above, via First Class Mail with sufficient postage attached thereto, in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Printed Name of Person Mailing Paper

REQUEST FOR A CERTIFICATE OF CORRECTION UNDER 37 CFR § 1.322

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 CFR § 1.322 of the Rules of Practice, which implement 35 USC § 254, the Patent and Trademark Office is respectfully requested to issue a Certificate of Correction in the above-identified patent. It is certified that errors appear in the above-identified patent as shown in the attached Certificate of Correction. Applicant certifies that the errors are of a minor character and were not the fault of Applicant. Since the changes necessary to correct these errors in the patent would not constitute new matter, and would not require re-examination, Applicant prays a Certificate of Correction will issue. Since errors were not the fault of Applicant, it is believed that there will not be a fee for this Certificate of Correction.

Respectfully submitted,

By _____
James A. Lamb
Attorney for Applicants
Registration No. 38,529
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Motorola, Inc.
Customer No.: 22917

PTO/SB/ 44 (07-03)
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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.: 6,819,181 B2

DATE: 11/16/2004

INVENTOR(S): Stengel et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

1. A method for signal isolation in electronic circuits, further comprising:

acquiring a signal of interest (SOI) at a local node;

coupling the SOI to a plurality of transmission paths, wherein each transmission path of the plurality of transmission paths has a phase and a delay distinct from others of the plurality of transmission paths;

setting the delay and phase of each transmission path of the plurality of transmission paths; and

combining the plurality of transmission paths at a remote node, wherein a signal at the remote node is created by summing a plurality of signals received on the plurality of transmission paths, said summation occurring in an in-phase manner in accordance with the selection of the delay and phase of each transmission path of the plurality of transmission paths, wherein the phase and delay of each transmission path are chosen to optimize an out-of-phase addition of a plurality of induced noise contributions that are essentially in-phase on the corresponding plurality of transmission paths.

12. A structure for signal isolation in electronic circuits, comprising:

a first node of a plurality of nodes of an input stage, said first node operable to receive a signal of interest (SOI);

the first node of the input stage coupled to a plurality of nodes of the plurality of nodes through a plurality of corresponding coupled elements, thereby creating a plurality of corresponding phased signals corresponding to the SOI;

each node of the plurality of nodes coupled to a plurality of transistive elements, said plurality of transistive elements operable to create a plurality of output signals at an output stage, said plurality of output signals proportional to the plurality of corresponding phased signals;

a plurality of remote nodes at the output stage coupled to the plurality of transistive

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.: 6,819,181 B2

DATE: 11/16/2004

INVENTOR(S): Stengel et al.

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1. A method for signal isolation in electronic circuits, further comprising:

acquiring a signal of interest (SOI) at a local node;

coupling the SOI to a plurality of transmission paths, wherein each transmission path of the plurality of transmission paths has a phase and a delay distinct from others of the plurality of transmission paths;

setting the delay and phase of each transmission path of the plurality of transmission paths; and

combining the plurality of transmission paths at a remote node, wherein a signal at the remote node is created by summing a plurality of signals received on the plurality of transmission paths, said summation occurring in an in-phase manner in accordance with the selection of the delay and phase of each transmission path of the plurality of transmission paths, wherein the phase and delay of each transmission path are chosen to optimize an out-of-phase addition of a plurality of induced noise contributions that are essentially in-phase on the corresponding plurality of transmission paths.

12. A structure for signal isolation in electronic circuits, comprising:

a first node of a plurality of nodes of an input stage, said first node operable to receive a signal of interest (SOI);

the first node of the input stage coupled to a plurality of nodes of the plurality of nodes through a plurality of corresponding coupled elements, thereby creating a plurality of corresponding phased signals corresponding to the SOI;

each node of the plurality of nodes coupled to a plurality of transistive elements, said plurality of transistive elements operable to create a plurality of output signals at an output stage, said plurality of output signals proportional to the plurality of corresponding phased signals;

a plurality of remote nodes at the output stage coupled to the plurality of transistive

a plurality of additive elements coupled to the plurality of remote nodes, wherein the plurality of remote nodes are combined by the plurality of additive elements to create a destination signal, said destination signal created by summing the plurality of corresponding phased signals in an in-phase manner, wherein each of the plurality of transistive elements is associated with an inductive element that couples an induced noise signal into the transistive element, and wherein the induced noise signals coupled into the plurality of transistive elements have essentially the same phase, and wherein the plurality of coupled elements, the plurality of additive elements, and the plurality of inductive elements are chosen to optimize an out-of phase addition of the induced noise signals.

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a plurality of additive elements coupled to the plurality of remote nodes, wherein the plurality of remote nodes are combined by the plurality of additive elements to create a destination signal, said destination signal created by summing the plurality of corresponding phased signals in an in-phase manner, wherein each of the plurality of transistive elements is associated with an inductive element that couples an induced noise signal into the transistive element, and wherein the induced noise signals coupled into the plurality of transistive elements have essentially the same phase, and wherein the plurality of coupled elements, the plurality of additive elements, and the plurality of inductive elements are chosen to optimize an out-of phase addition of the induced noise signals.

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